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10/053,198	01/17/2002	Chinnugounder Senthilkumar	10559/649001/P12971	2860

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EXAMINER
SHINGLETON, MICHAEL B

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 05/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
10-053,198	Senthilkumar et al.
Examiner	**Group Art Unit**
SHINGLETON	2817

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-22 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-7, 10-20 and 22 is/are rejected.

☒ Claim(s) 8, 9 and 21 is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: "Low power amplifier operating in the weak inversion region".

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The "first portion" and the "second portion" does not seem to appear in the specification. The examiner notes that the specification describes a "leg" and "another leg" for the self-bias circuit 106 (See page 2 of the specification). If these "legs" are the "first and second portions" of the claims, it is important to note that "[t]he use of a confusing variety of terms for the same thing should not be permitted" (See MPEP 608.01(o)).

The disclosure is objected to because of the following informalities: The specification does not identify which component of the "second portion" provides for a negative feedback in response to a change in the amount of current flowing through the "second portion". As noted above the examiner has not been able to find the terminology "second portion" in the original specification and it is assumed for examining purposes to be one of the "legs" of the self-bias circuit 106.

Appropriate correction is required.

Drawings

The drawings are objected to because the identification of the source and drain terminals of the transistors is not presented in the drawings even though the claims recite these specific connections. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty

defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 10, 13-16 are rejected under 35 U.S.C. 102(e) as anticipated by Jansson 6,278,338 (Jansson) as evidenced by Vittoz et al. "CMOS Analog Integrated Circuits Based on Weak Inversion Operation" (Vittoz).

Figure 3 and columns 3 and 4 of Jansson set forth an integrated crystal oscillator apparatus. Jansson states: "FIG 3 is described in more detail in the Vittoz article". Thus in accordance with MPEP 2131.01, this 35 USC 102 rejection is based upon both Jansson and Vittoz. Vittoz merely helps explain the meaning of the referenced and unreferenced terminology used in the specification and drawings of Jansson and shows that the characteristics not disclosed in Jansson are inherent. Figure 3 of Jansson does not give reference numerals for each and every element in Figure 3. Therefore, in order for the following rejection to accurately point to item by item in the claims of the instant application and for applicant's ease of understanding, the following copy of Figure 3 of Jansson is provided with reference symbols and this rejection refers to these reference symbols.

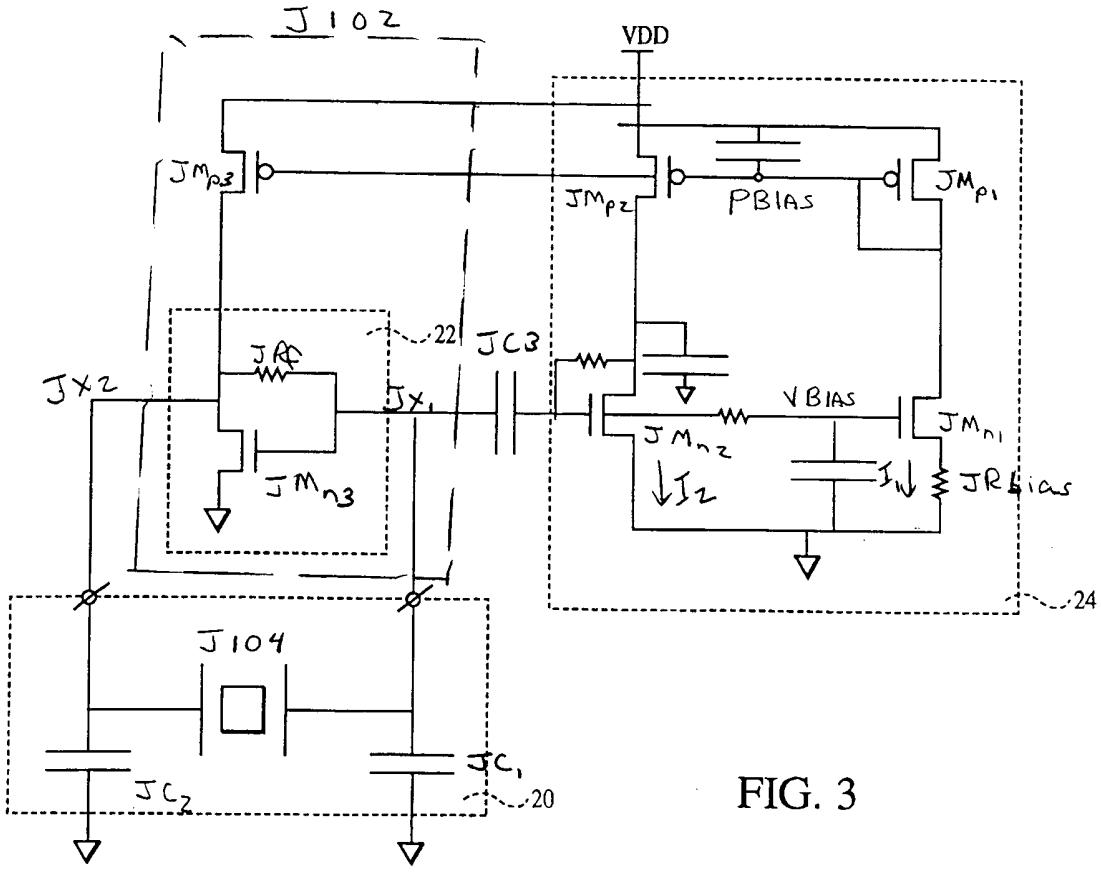


FIG. 3

Note that while Figure 3 of Jansson is not clear on whether the line "PBIAS" directly connects to all the gates of JMp1, JMp2, and JMp3. It is clearly from Vittoz that such is the case.

Figure 3 of Jansson as evidenced by Vittoz discloses an "apparatus" having an oscillator circuit J100 that is for generating "an oscillating signal" at the terminal JX1. This oscillator circuit J100 has an inverting amplifier J102 and a resonator J104. The crystal resonator J104 has two terminals, JX1 and JX2, that are connected to input and output terminals, respectively, of inverting amplifier J102, as is clearly shown in Figure 3 of Jansson as evidenced by Vittoz (Also note page 4, lines 15-17 of the instant application and at least claim 2 of the instant application.). Jansson as evidenced by Vittoz also includes a feedback resistor JRf that feeds back a portion of the amplified oscillating signal to the input of the amplifier as clearly shown in Figure 3 of Jansson as evidenced by Vittoz. Jansson as evidenced by Vittoz also provides a "bias circuit" 24. Note this arrangement produces a relatively constant current I1 flowing through relatively constant current source JMp1 and JMn1, and a relatively constant current I2 flowing through relatively constant current source JMp2 and JMn2 because of the current mirror arrangement of these transistors (Also see Figure 9 of Vittoz). Since all of the structure of the bias circuit 106 of the instant invention is clearly present in Figure 3 of Jansson, the "relatively constant current source", noted above, is "configured to create a relatively constant bias voltage (PBIAS) to bias the amplifier in an operating state that can sustain the oscillating signal" as is inherent in Jansson as evidenced by Vittoz. While Jansson does not identify the operation region of the transistors of the bias circuit and the transistors of the inverting amplifier when an "operation state" is obtained, the transistors of Jansson as evidenced by Vittoz are operated in the weak inversion region when an "operation state" is obtained as evidenced by Vittoz. In particular note page 229 of Vittoz. The "weak inversion" region is also well known in the art as the "sub-threshold region". The relatively constant current source JMp1, JMn1, JMp2, and JMn2 has a first portion JMp1 and JMn1 that produces a relatively constant current I1 and a second portion JMp2 and JMn2 that produces a relatively constant current I2. The "first current" is I1 and the "second current" is I2. Because of the action of the current mirror arrangement of the transistors of Jansson as evidenced by Vittoz, Jansson as evidenced by Vittoz inherently produces a first current that is a substantially fixed ratio to the second current. Also because of the action of the current mirror arrangement of the transistors of Jansson as evidenced by Vittoz, Jansson as evidenced by Vittoz inherently provides the direct current bias voltage on the node "PBIAS" that is electrically connected to the inverting amplifier J102 as clearly shown in Figure 3 of Jansson and also because of this action of the current mirror arrangement of Jansson as evidenced by Vittoz this bias voltage has a "predefined" relationship with the current flowing through the first portion. The specification does not identify which

component provides for "negative feedback in response to a change in the amount of current flowing through the second portion", however, because Jansson as evidenced by Vittoz has all the same structure for what the examiner believes is the "second portion" (See the above lack of antecedent basis in the specification for this terminology.) one of these components inherently provides for "negative feedback in response to a change in the amount of current flowing through the second portion".

The apparatus of Jansson as evidenced by Vittoz is silent on the statement of intended use as presented in claims like base claim 1. Namely, claim 1 of the instant invention states in the preamble that the invention claimed is "for generating a clock signal". This appears only in the preamble of the claim and accordingly Jansson as evidenced by Vittoz is seen as anticipating the claimed invention. However, column 3, around line 56 of Jansson clearly recognizes the use of this oscillator in a digital watch. It is well known that a digital watch uses such an oscillator as a clocking mechanism to control the movement of the hands of the watch or the selection of the appropriate digit to be displayed. Thus the oscillator of Jansson as evidenced by Vittoz inherently generates a clock signal. All constant frequency oscillators inherently generate a "clock" signal. Since the clock oscillator of Jansson as evidenced by Vittoz generates its clock signal in "real time" the oscillator of Jansson as evidenced by Vittoz is a "real time clock oscillator circuit".

As noted above the relatively constant current source 24 of Jansson as evidenced by Vittoz produces a bias voltage PBIAS. This bias voltage is applied at the node where PBIAS is shown in the above Figure. Thus, Jansson as evidenced by Vittoz clearly includes a "bias node" PBIAS and the relatively constant current source 24 is configured to create the bias voltage PBIAS at the bias node PBIAS. As recognized by Jansson as evidenced by Vittoz the capacitor JC3 in combination with the transistors of element 24 and voltage source Vdd provides for an amplitude regulation during start-up and provides an excitation circuit as recognized specifically on page 229 of Vittoz. This excites the bias circuit to start operation and provide a stable bias voltage. Thus the capacitor JC3 in combination with the transistors of element 24 and the voltage source Vdd forms an "excitation circuit".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject

matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jansson 6,278,338 (Jansson) as evidenced by Vittoz et al. "CMOS Analog Integrated Circuits Based on Weak Inversion Operation" (Vittoz) in view of Volk 6,191,662 (Volk).

All the same reasoning as applied in the rejection of claims 1-7, 10 and 13-16 above and the following: Jansson as evidenced by Vittoz does not have an inhibit circuit that is configured to inhibit the excitation when the bias circuit is capable of sustaining the bias voltage at a predetermined level.

Volk discloses that in an excitation circuit 400 that includes an inhibit circuit that shuts off the excitation circuit when the bias is capable of sustaining the bias voltage at a set level (See column 4, lines 41-46). Volk also teaches that the addition of an excitation circuit also "kicks" the oscillator into oscillation (See column 4, around line 3).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Jansson as evidenced by Vittoz with an excitation circuit that "kicks" the oscillator and inhibits the excitation when the bias circuit is capable of sustaining the bias voltage at a predetermined level so as to insure that the oscillator starts oscillating and to save energy by disabling this excitation circuit after the excitation circuit has completed its function as all taught by Volk.

Claims 12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jansson 6,278,338 (Jansson) as evidenced by Vittoz et al. "CMOS Analog Integrated Circuits Based on Weak Inversion Operation" (Vittoz) in view of Millman.

All the same reasoning as presented in the above rejection of claims 1-7, 10 and 13-16 and the following:

Jansson as evidenced by Vittoz clearly discloses the relatively constant current source having a first PMOS transistor JM_{p1}, a second PMOS transistor JM_{p2}, a first NMOS transistor JM_{n1}, a second NMOS transistor JM_{n2}, and a resistor JRbias having a first end and a second end, each of the transistors having a gate node, a source node and a drain node (Note that the transistors are MOSFETs). Jansson as evidenced by Vittoz also clearly shows a drain/source node of the first PMOS transistor JM_{p1} being

coupled to the drain/source node of the first NMOS transistor JM_{n1}. Jansson as evidenced by Vittoz also clearly shows the drain/source node of the second PMOS transistor JM_{p2} being coupled to the drain/source node of the second NMOS transistor JM_{n2}. Jansson as evidenced by Vittoz also clearly shows the gate nodes of the first and second NMOS transistors being coupled to the drain/source node of the second NMOS transistor JM_{n2}. Jansson as evidenced by Vittoz also clearly shows the source/drain node of the first NMOS transistor JM_{n1} being coupled to the first end of the resistor JRbias and the relatively constant bias voltage PBIAS being created at the gate nodes of the first and second PMOS transistors as noted above. While it is clear that the "drain/source" nodes of Jansson as evidenced by Vittoz are either the drain or the source, Jansson as evidenced by Vittoz is silent on the specific naming of these nodes.

Millman specifically states that "[s]ince the FET is a symmetrical device either end of the channel may be used as the source". Thus either end of the channel can be named the source or the drain due to the bi-directional nature of the device.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to set forth that the node directly connected between the first PMOS and first NMOS transistors be called the drains of the first PMOS and NMOS transistors and to set forth that the node directly connected between the second PMOS and second NMOS transistors be called the drains of the second PMOS and NMOS transistors because a field effect transistor is a bi-directional device and accordingly either end of the channel may be used as the source as taught by Millman.

Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walsh et al. 5,848,253 (Walsh) in view of Jansson 6,278,338 (Jansson) as evidenced by Vittoz et al. "CMOS Analog Integrated Circuits Based on Weak Inversion Operation" (Vittoz).

Walsh discloses the basic computer arrangement Note Figure 29-1 shows the processor "CPU", the memory "adapted to store data", a "chipset" for managing data transfers between the memory and the processor and an oscillator. Walsh is silent on the exact structure of the oscillator, i.e. clock.

Jansson as evidenced by Vittoz shows the specific structure of a conventional clock oscillator. Specifically, Figure 3 and columns 3 and 4 of Jansson set forth an integrated crystal oscillator apparatus. Jansson states: "FIG 3 is described in more detail in the Vittoz article". Thus in accordance with MPEP 2131.01, this 35 USC 102 rejection is based upon both Jansson and Vittoz. Vittoz merely helps explain the meaning of the referenced and unreferenced terminology used in the specification and drawings of Jansson and shows that the characteristics not disclosed in Jansson are inherent. Figure 3 of Jansson does not give reference numerals for each and every element in Figure 3. Therefore, in order for the following rejection to accurately point to item by item in the claims of the instant application and for applicant's ease of understanding, the following copy of Figure 3 of Jansson is provided with reference symbols and this rejection refers to these reference symbols.

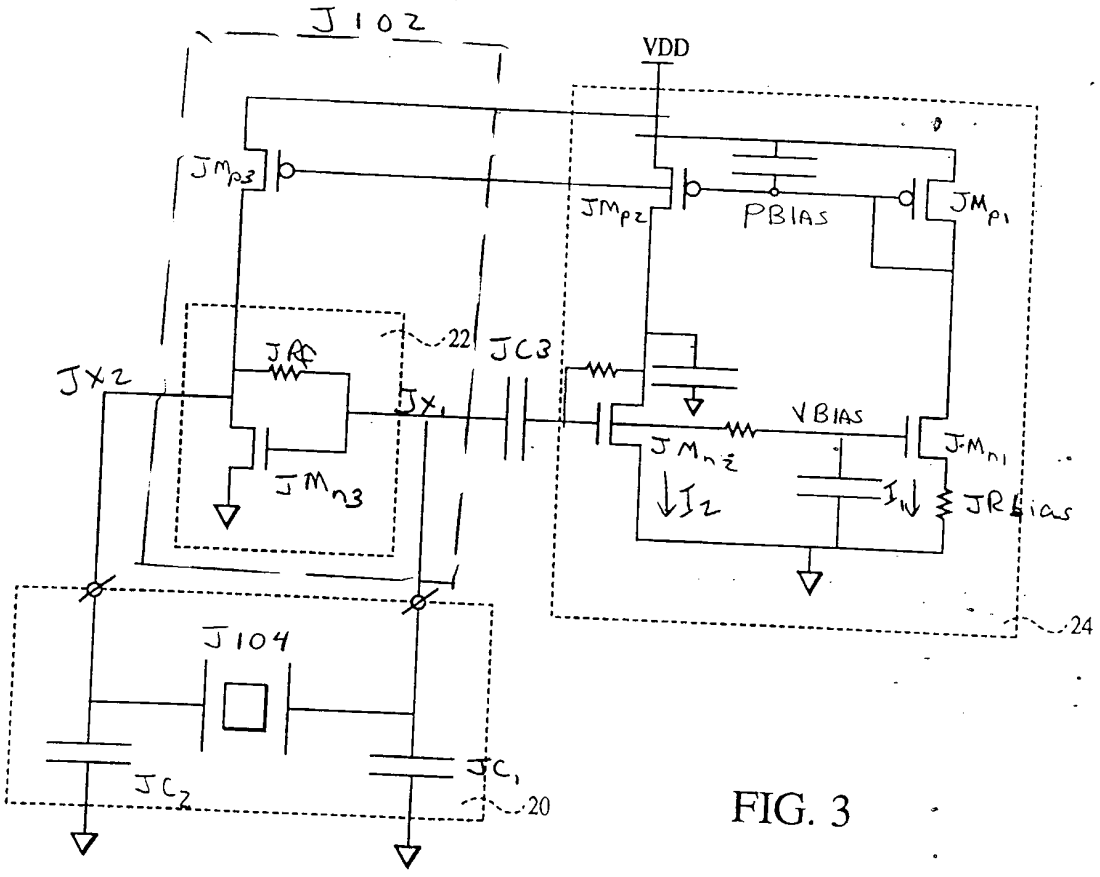


FIG. 3

Note that while Figure 3 of Jansson is not clear on whether the line "PBIAS" directly connects to all the gates of JMp1, JMp2, and JMp3. It is clearly from Vittoz that such is the case.

Figure 3 of Jansson as evidenced by Vittoz discloses an "apparatus" having an oscillator circuit J100 that is for generating "an oscillating signal" at the terminal JX1. This oscillator circuit J100 has an inverting amplifier J102 and a resonator J104. The crystal resonator J104 has two terminals, JX1 and JX2, that are connected to input and output terminals, respectively, of inverting amplifier J102, as is clearly shown in Figure 3 of Jansson as evidenced by Vittoz (Also note page 4, lines 15-17 of the instant application and at least claim 2 of the instant application.). Jansson as evidenced by Vittoz also includes a feedback resistor JRf that feeds back a portion of the amplified oscillating signal to the input of the amplifier as clearly shown in Figure 3 of Jansson as evidenced by Vittoz. Jansson as evidenced by Vittoz also provides a "bias circuit" 24. Note this arrangement produces a relatively constant current I1 flowing through relatively constant current source JMp1 and JMn1, and a relatively constant current I2 flowing through relatively constant current source JMp2 and JMn2 because of the current mirror arrangement of these transistors (Also see Figure 9 of Vittoz). Since all of the structure of the bias circuit 106 of the instant invention is clearly present in Figure 3 of Jansson, the "relatively constant current source", noted above, is "configured to create a relatively constant bias voltage (PBIAS) to bias the amplifier in an operating state that can sustain the oscillating signal" as is inherent in Jansson as evidenced by Vittoz. While Jansson does not identify the operation region of the transistors of the bias circuit and the transistors of the inverting amplifier when an "operation state" is obtained, the transistors of Jansson as evidenced by Vittoz are operated in the weak inversion region when an "operation state" is obtained as evidenced by Vittoz. In particular note page 229 of Vittoz. The "weak inversion" region is also well known in the art as the "sub-threshold region". The relatively constant current source JMp1, JMn1, JMp2, and JMn2 has a first portion JMp1 and JMn1 that produces a relatively constant current I1 and a second portion JMp2 and JMn2 that produces a relatively constant current I2. The "first current" is I1 and the "second current" is I2. Because of the action of the current mirror arrangement of the transistors of Jansson as evidenced by Vittoz, Jansson as evidenced by Vittoz inherently produces a first current that is a substantially fixed ratio to the second current. Also because of the action of the current mirror arrangement of the transistors of Jansson as evidenced by Vittoz, Jansson as evidenced by Vittoz

inherently provides the direct current bias voltage on the node "PBIAS" that is electrically connected to the inverting amplifier J102 as clearly shown in Figure 3 of Jansson and also because of this action of the current mirror arrangement of Jansson as evidenced by Vittoz this bias voltage has a "predefined" relationship with the current flowing through the first portion. The specification does not identify which component provides for "negative feedback in response to a change in the amount of current flowing through the second portion", however, because Jansson as evidenced by Vittoz has all the same structure for what the examiner believes is the "second portion" (See the above lack of antecedent basis in the specification for this terminology.) one of these components inherently provides for "negative feedback in response to a change in the amount of current flowing through the second portion".

The apparatus of Jansson as evidenced by Vittoz is silent on the statement of intended use as presented in claims like base claim 1. Namely, claim 1 of the instant invention states in the preamble that the invention claimed is "for generating a clock signal". This appears only in the preamble of the claim and accordingly Jansson as evidenced by Vittoz is seen as anticipating the claimed invention. However, column 3, around line 56 of Jansson clearly recognizes the use of this oscillator in a digital watch. It is well known that a digital watch uses such an oscillator as a clocking mechanism to control the movement of the hands of the watch or the selection of the appropriate digit to be displayed. Thus the oscillator of Jansson as evidenced by Vittoz inherently generates a clock signal. All constant frequency oscillators inherently generate a "clock" signal. Since the clock oscillator of Jansson as evidenced by Vittoz generates its clock signal in "real time" the oscillator of Jansson as evidenced by Vittoz is a "real time clock oscillator circuit".

As noted above the relatively constant current source 24 of Jansson as evidenced by Vittoz produces a bias voltage PBIAS. This bias voltage is applied at the node where PBIAS is shown in the above Figure. Thus, Jansson as evidenced by Vittoz clearly includes a "bias node" PBIAS and the relatively constant current source 24 is configured to create the bias voltage PBIAS at the bias node PBIAS. As recognized by Jansson as evidenced by Vittoz the capacitor JC3 in combination with the transistors of element 24 and voltage source Vdd provides for an amplitude regulation during start-up and provides an excitation circuit as recognized specifically on page 229 of Vittoz. This excites the bias circuit to start operation and provide a stable bias voltage. Thus the capacitor JC3 in combination with the transistors of element 24 and the voltage source Vdd forms an "excitation circuit".

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the conventional clock oscillator for the generic clock oscillator

of Walsh because, as the reference is silent as the specific structure that makes up the clock oscillator, any art-recognized equivalent clock oscillator structure would have been usable therefore such as the well-known, conventional clock oscillator as disclosed by Jansson as evidenced by Vittoz.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walsh in view of Jansson 6,278,338 (Jansson) as evidenced by Vittoz et al. "CMOS Analog Integrated Circuits Based on Weak Inversion Operation" (Vittoz) as applied to claims 18-20 above, and further in view of Millman.

All the same reasoning as applied in the rejection of claims 18-20 above and the following:

Jansson as evidenced by Vittoz clearly discloses the relatively constant current source having a first PMOS transistor JM_{p1}, a second PMOS transistor JM_{p2}, a first NMOS transistor JM_{n1}, a second NMOS transistor JM_{n2}, and a resistor JRbias having a first end and a second end, each of the transistors having a gate node, a source node and a drain node (Note that the transistors are MOSFETs). Jansson as evidenced by Vittoz also clearly shows a drain/source node of the first PMOS transistor JM_{p1} being coupled to the drain/source node of the first NMOS transistor JM_{n1}. Jansson as evidenced by Vittoz also clearly shows the drain/source node of the second PMOS transistor JM_{p2} being coupled to the drain/source node of the second NMOS transistor JM_{n2}. Jansson as evidenced by Vittoz also clearly shows the gate nodes of the first and second NMOS transistors being coupled to the drain/source node of the second NMOS transistor JM_{n2}. Jansson as evidenced by Vittoz also clearly shows the source/drain node of the first NMOS transistor JM_{n1} being coupled to the first end of the resistor JRbias and the relatively constant bias voltage PBIAS being created at the gate nodes of the first and second PMOS transistors as noted above. While it is clear that the "drain/source" nodes of Jansson as evidenced by Vittoz are either the drain or the source, WALSH and Jansson as evidenced by Vittoz are silent on the specific naming of these nodes.

Millman specifically states that "[s]ince the FET is a symmetrical device either end of the channel may be used as the source". Thus either end of the channel can be named the source or the drain due to the bi-directional nature of the device.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to set forth that the node directly connected between the first PMOS and first NMOS transistors be called the drains of the first PMOS and NMOS transistors and to set forth that the node directly connected between the second PMOS and second NMOS transistors be called the drains of the second PMOS and

NMOS transistors because a field effect transistor is a bi-directional device and accordingly either end of the channel may be used as the source as taught by Millman.

Allowable Subject Matter

Claims 8, 9 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record fails to describe or suggest disposing the claimed bias circuit arrangement within an integrated circuit and connecting this claimed bias circuit arrangement to the claimed amplifier arrangement only through the bias node.

Conclusion

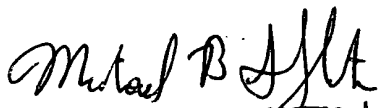
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Okutsu et al. discloses a CMOS circuit used with a crystal oscillation circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is 703-308-4903. The examiner can normally be reached on Monday-Thursday from 8:30 to 4:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (703) 308-4909. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MBS
May 8, 2003



MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817